In Example 9, the one or more transformation execution engines of at least one of Examples 1-8 include a second transformation execution engine configured to execute sixteen bit instructions and data.

In Example 10, the one or more transformation execution engines of at least one of Examples 1-9 include a transformation execution engine configured to execute thirty-two bit instructions and data.

In Example 11 a computer is configured to receive instructions and data in a Von Neumann architecture format, convert the instructions and data to a Harvard architecture format, and execute the instructions and data in the Harvard architecture format.

In Example 12, the computer of at least one of Examples 1-11 includes a harvardizer configured to convert the instructions and data to the Harvard architecture format, wherein the Harvard architecture format includes separate data and instructions and the Von Neumann architecture format includes comingled data and instructions.

In Example 13, the computer of at least one of Examples 1-12 includes one or more transformation execution engines configured to execute the instructions and data in the Harvard architecture format.

In Example 14, the computer of at least one of Examples 1-13 includes one or more encryptors configured to encrypt the converted instructions and data.

In Example 15, the computer of at least one of Examples 1-14 includes an instruction memory configured to receive encrypted instructions from the one or more encryptors.

In Example 16, the computer of at least one of Examples 1-15 includes a data memory configured to receive encrypted data from the one or more encryptors.

In Example 17, the computer of at least one of Examples 1-16 includes one or more decryptors configured to decrypt the encrypted instructions and data and send the decrypted instructions and data to a transformation execution engine of the one or more transformation execution engines.

In Example 18 a method includes receiving, at a computer, instructions and data in a Von Neumann format, converting the instructions and data to a Harvard format, and executing the instructions and data in the Harvard format.

In Example 19, the method of at least one of Examples 1-18 includes encrypting the converted instructions and data.

In Example 20, the method of at least one of Examples 1-19 includes sending the encrypted instructions to an instruction memory.

In Example 21, the method of at least one of Examples 1-20 includes sending the encrypted data to a data memory, the data memory physically separate from the instruction memory.

In Example 22, the method of at least one of Examples 1-21 includes decrypting the encrypted instructions and data.

In Example 23, the method of at least one of Examples 1-22 includes sending the decrypted instructions to one or more processors on an instruction signal path and the decrypted data to the one or more processors on a data signal path, the data signal path physically separate from the instruction signal path.

In this document, the terms "a" or "an" are used, as is common in patent documents, to include one or more than one, independent of any other instances or usages of "at least one" or "one or more." In this document, the term "or" is used to refer to a nonexclusive or, such that "A or B" includes "A but not B," "B but not A," and "A and B," unless otherwise indicated. In this document, the terms "including" and "in which" are used as the plain-English equivalents of the respective terms "comprising" and "wherein." Also, in the following claims, the terms "including" and "comprising" are open-ended, that is, a system, device, article, composition, formulation, or process that includes elements in addition to those listed after such a term in a claim are still deemed to fall within the scope of that claim. Moreover, in the following claims, the terms "first," "second," and "third," etc. are used merely as labels, and are not intended to impose numerical requirements on their objects.

Although an embodiment has been described with reference to specific example embodiments, it will be evident that various modifications and changes may be made to these embodiments without departing from the broader spirit and scope of the invention. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense. The accompanying drawings that form a part hereof, show by way of illustration, and not of limitation, specific embodiments in which the subject matter may be practiced. The embodiments illustrated are described in sufficient detail to enable those skilled in the art to practice the teachings disclosed herein. Other embodiments may be utilized and derived therefrom, such that structural and logical substitutions and changes may be made without departing from the scope of this disclosure. This Detailed Description, therefore, is not to be taken in a limiting sense, and the scope of various embodiments is defined only by the appended claims, along with the full range of equivalents to which such claims are entitled.

Such embodiments of the disclosed subject matter may be referred to herein, individually and/or collectively, by the term "invention" merely for convenience and without intending to voluntarily limit the scope of this application to any single invention or inventive concept if more than one is in fact disclosed. Thus, although specific embodiments have been illustrated and described herein, it should be appreciated that any arrangement calculated to achieve the same purpose may be substituted for the specific embodiments shown. This disclosure is intended to cover any and all adaptations or variations of various embodiments. Combinations of the above embodiments, and other embodiments not specifically described herein, will be apparent to those of skill in the art upon reviewing the above description.

The functions or algorithms described herein are implemented in hardware, software, or a combination of software and hardware in some embodiments. The software can comprise computer executable instructions stored on computer readable media such as memory or other type of storage devices. Further, described functions can correspond to modules, which can be software, hardware, firmware, or any combination thereof. Multiple functions are performed in one or more modules as desired, and the embodiments described are merely embodiments. The software is executed on a digital signal processor, ASIC, microprocessor, or other type of processor operating on a system, such as a personal computer, server, a router, or other device capable of processing data including network interconnection devices.

Some embodiments implement the functions in two or more specific interconnected hardware modules or devices with related control and data signals communicated between and through the modules, or as portions of an application-specific integrated circuit. Thus, process flows can be applicable to software, firmware, and hardware implementations.

Systems and methods of the present disclosure can be implemented on a mobile device as a mobile application, web-based application, on a desktop computer as a computer application, or a combination thereof. A mobile application can operate on a Smartphone, tablet computer, portable digital assistant (PDA), ruggedized mobile computer, or other